STIC Search Report
EIC 2800

STIC Database Tracking Number: 202848

TO: Andrew Tran **Location: JEF 7A71** **Art Unit: 2824** ~~**Thursday, May 22, 2003**~~ at **Case Serial Number: 09/932467**	**From: Lucy Park** **Location: STIC-EIC2800** **JEF 4B59** **Phone: 272-8667** **Email: lucy.park@uspto.gov**

Search Notes

Examiner Tran,

Attached are search results for your STIC search request. I have flagged the records that looked most relevant, but please review all of the results. Please don't hesitate to contact me if you have any questions about the search or would like me to refocus it.

Thanks,
Lucy

Lucy Park
Patent Searcher
ASRC Aerospace
STIC-EIC 2800

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File 344:Chinese Patents Abs Jan 1985-2006/Jan
         (c) 2006 European Patent Office
File 347:JAPIO Dec 1976-2005/Dec(Updated 060404)
         (c) 2006 JPO & JAPIO
File 350:Derwent WPIX 1963-2006/UD=200662
         (c) 2006 The Thomson Corporation
File 371:French Patents 1961-2002/BOPI 200209
         (c) 2002 INPI.  All rts. reserv.

Set     Items   Description
S1     966437   MATRIX OR MATRICES OR ARRAY? ? OR TABLE? ? OR ROW?
?(3N)COLUMN? ?
S2    1244865   ADDRESS???? OR POINTER? ? OR REFERENCE? ? OR LOCATION?
? OR LOCATOR? ?
S3    2694602   LAYER??? OR SUBLAYER??? OR MULTILAYER? ? OR BAND? ? OR
STRATUM OR STRATA
S4    1850199   SWITCH??? OR GATE OR GATES
S5     225400   S4(3N)(CONNECT???? OR LINK??? OR CHAIN??? OR
ATTACH?????)
S6     656630   SERIAL? OR SEQUENTIAL? OR SUCCESSIVE?
S7        128   VIRTUAL??(3N)COLUMN? ?
S8     191406   S4(3N)(TWO OR SECOND OR 2ND OR DUAL OR TWIN OR COUPLE
OR ANOTHER OR ADDITIONAL OR DIFFERENT)
S9       1159   S1 AND S2(3N)S3
S10         1   S9 AND S5(3N)S6
S11        61   S9 AND S5
S12         1   S11 AND S7
S13         0   S12 NOT S10
S14        19   S11 AND S8
S15        14   S14 NOT AD=20000817:20030817/PR
S16        13   S15 NOT AD=20030817:20061002/PR
S17        13   S16 NOT S10
S18         2   S9 AND S7
S19         1   S18 NOT (S10 OR S17)
S20      9332   S2(3N)S3
S21       306   S20 AND S4 AND S1
S22        23   S21 AND IC=G06F
S23        22   S22 NOT (S10 OR S17 OR S19)
S24        13   S23 NOT AD=20000817:20030817/PR
S25         9   S24 NOT AD=20030817:20061002/PR
S26        63   S7 AND S1
S27        29   S26 AND S2
S28        27   S27 NOT (S10 OR S17 OR S19 OR S23)
S29        23   S28 NOT AD=20000817:20030817/PR
S30        23   S29 NOT AD=20030817:20061002/PR
S31       253   S20 AND S8
S32    229448   SIGNAL?(3N)(TWO OR SECOND OR 2ND OR DUAL OR TWIN OR
COUPLE OR ANOTHER OR ADDITIONAL OR DIFFERENT)
S33        23   S31 AND S32
S34        22   S33 NOT (S10 OR S17 OR S19 OR S23 OR S28)
S35        19   S34 NOT AD=20000817:20030817/PR
S36        17   S35 NOT AD=20030817:20061002/PR
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30/5/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

05015258 **Image available**
IMAGE PRINTER

PUB. NO.: 07-307858 [JP 7307858 A]
PUBLISHED: November 21, 1995 (19951121)
INVENTOR(s): INOUE HIDEAKI
APPLICANT(s): CASIO COMPUT CO LTD [350750] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-100073 [JP 94100073]
FILED: May 13, 1994 (19940513)
INTL CLASS: [6] H04N-001/387; B41J-002/485; B41J-005/30; G06T-003/00
JAPIO CLASS: 44.7 (COMMUNICATION -- Facsimile); 29.4 (PRECISION INSTRUMENTS -- Business Machines); 45.9 (INFORMATION PROCESSING -- Other)
JAPIO KEYWORD:R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessers)

ABSTRACT

PURPOSE: To attain the rotation of an image, staggered print and magnification at an optional magnification rate with simple circuit configuration in a prescribed processing time.

CONSTITUTION: A **virtual column** generating circuit 13 and a virtual row generating circuit 14 set a virtual coordinate space comprising a 16-bit **virtual column** coordinate and a 15-bit virtual row coordinate, and magnified printing is implemented by generating image data with synthesis to a virtual coordinate space comprising low-order 7 bits of a **column** coordinate and a **row** coordinate corresponding to the **address** space of an image memory 16 comprising 9-bit column **addresses** and 8-bit row **addresses** by means of high-order 9 bits of the column coordinate and high-order 8 bits of the row **addresses** . When image is not rotated by 90 deg., main scanning is applied in the X axis direction of the tentative coordinate and subscanning is applied in the Y axis direction, and when image is rotated by 90 deg., main scanning is applied in the inverse Y axis direction of the tentative coordinate and subscanning is applied in the X axis direction. When even order number of subscanning is implemented, the main scanning is implemented usually and when odd number order of subscanning is implemented, the main scanning is conducted while a read start position is deviated by a half of the main scanning interval. The scale of the X and Y axes of the tentative coordinate is set to be 1:.square root.3. The image is printed in a staggered shape so that the aspect ratio of one picture element is 1:.square root.3.

36/5/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0013960715 - Drawing available
WPI ACC NO: 2004-141379/200414
XRPX Acc No: N2004-112807
Memory module for computer memory system, includes skew-reducing locations arranged transverse to long axis of module substrate, such that signals routed in layers are switched **to** different signal **routing layers**
Patent Assignee: RAMBUS INC (RAMB-N)
Inventor: KOLLIPARA R T
Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
US 6681338	B1	20040120	US 2000599091	A	20000621	200414 B

Priority Applications (no., kind, date): US 2000599091 A 20000621

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 6681338	B1	EN	14	6	

Alerting Abstract US B1
NOVELTY - The module includes signal routing layers (504,506) to which several memory devices (502) such as dynamic RAM (DRAM) supported by a module substrate, are connected. Several skew-reducing locations are arranged in a line transverse to the long axis of the module substrate, such that signals routed in the routing layers are **switched** to **different signal** routing layers.
DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

1.high frequency system;

2.skew reducing, signal routing method; and

3.skew reduced memory module forming method.

USE - For computer memory system such as dual in-line memory module (DIMM) system and Rambus-in-line memory module (RIMM) system.
ADVANTAGE - The propagation delay differences between the signal groups is effectively reduced by arranging the skew-reducing locations for switching the signals between the **different signal** routing layers.
DESCRIPTION OF DRAWINGS - The figure shows the schematic view of the memory module along with the sectional views.
500 module
502 memory devices
504,506 signal routing layers
508 via
Title Terms/Index Terms/Additional Words: MEMORY; MODULE; COMPUTER; SYSTEM; SKEW; REDUCE; LOCATE; ARRANGE; TRANSVERSE; LONG; AXIS; SUBSTRATE; SIGNAL; ROUTE; LAYER; SWITCH

Class Codes
International Classification (Main): G06F-001/04
US Classification, Issued: 713503000, 716012000, 711105000

File Segment: EPI;
DWPI Class: T01; U22
Manual Codes (EPI/S-X): T01-H01B3; T01-K; U22-D01A1

30/5/8 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0009445835 - Drawing available
WPI ACC NO: 1999-384879/
XRPX Acc No: N1999-288233
Content addressable **memory cell structure for flash memory** array
Patent Assignee: WAFERSCALE INTEGRATION INC (WAFE-N)
Inventor: ROY A
Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
US 5917743	A	19990629	US 1997953714	A	19971017	199932 B

Priority Applications (no., kind, date): US 1997953714 A 19971017

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 5917743	A	EN	5	2	

Alerting Abstract US A
NOVELTY - A cam cell (8) has four multiple **row columns** of **virtual** ground flash cells (10) with diffusion lines (12) provided between cells of neighboring columns. Two diffusion lines (12A,12B) which are clad with metal having contacts (14) at both ends are provided between predetermined columns (B,C,A,D) to function as bit line and read line.
DESCRIPTION - Column C is used to store the bit of interest. Columns (B,D) are not programmed and column A has field on thick oxides in the cells.
USE - For flash memory **array** .
ADVANTAGE - CAM cells are independently accessed. Enables accessing cam cells simultaneously since same voltage is applied to bit lines and read lines.
DESCRIPTION OF DRAWINGS - The figure shows the circuit diagram of CAM cell.
8 Cam cell
10 Flash cell
12,12A,12B Diffusion lines
14 Contact
A-D Column

Title Terms/Index Terms/Additional Words: CONTENT; **ADDRESS** ; MEMORY; CELL; STRUCTURE; FLASH; **ARRAY**

Class Codes
International Classification (Main): G11C-007/00
US Classification, Issued: 365049000, 365185160

File Segment: EPI;
DWPI Class: U13; U14
Manual Codes (EPI/S-X): U13-C04B2; U14-A03B7; U14-A05

30/5/9 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0009124639 - Drawing available
WPI ACC NO: 1999-044936/199904
XRPX Acc No: N1999-032834
Programmable logic array **integrated circuit device - has multiplexer circuitry to access data in memory area in response to transpose enable signal for selection between non- transposed and transposed mode**
Patent Assignee: ALTERA CORP (ALTE-N)
Inventor: LEE F F
Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
US 5844854	A	19981201	US 199626288	P	19960918	199904 B
			US 1996759304	A	19961202	

Priority Applications (no., kind, date): US 199626288 P 19960918; US 1996759304 A 19961202

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 5844854	A	EN	22	11	Related to Provisional US 199626288

Alerting Abstract US A

The device (10) includes a memory **array** (40) having multiple **rows** and **columns** of memory cell for storing data. A multiplexer circuitry accesses the data in the memory **array** in response to transpose enable signal for selecting between a non- transposed mode and a transposed mode in which the memory **array** is accessed using non-transposed and transposed words respectively. The transposed word contains data bits corresponding to cells in **virtual columns** while the non- transposed words contains data bits corresponding to cells in virtual rows.

ADVANTAGE - Enables modification of depth and width of memory **array** . Provides improved arrangement for accessing data in programmable logic device memory **array** .

Title Terms/Index Terms/Additional Words: PROGRAM; LOGIC; **ARRAY** ; INTEGRATE; CIRCUIT; DEVICE; MULTIPLEX; ACCESS; DATA; MEMORY; AREA; RESPOND; TRANSPOSE; ENABLE; SIGNAL; SELECT; NON; MODE

Class Codes
International Classification (Main): G11C-013/00
US Classification, Issued: 361230010, 365230030

File Segment: EPI;
DWPI Class: U13; U14
Manual Codes (EPI/S-X): U13-C04C; U14-A08A

25/5/8 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0003813554
WPI ACC NO: 1986-267088/
Addressing matrix array **ferroelectric liquid crystal cell - using parallel entry of balanced bipolar data pulses on one set of electrodes to cooperate with bipolar strobe pulses**
Patent Assignee: INT STANDARD ELECTRIC CORP (INTT); STC PLC (STTE)
Inventor: AYLIFFE P J; DAVEY A B; ZELISSE J K
Patent Family (5 patents, 6 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
GB 2173337	A	19861008	GB 19858713	A	19850403	198641	B
EP 197743	A	19861015	EP 1986302381	A	19860401	198642	E
AU 198655369	A	19861009				198647	E
US 4728947	A	19880301	US 1986847331	A	19860402	198812	E
GB 2173337	B	19890111	GB 19858713	A	19850403	198902	E

Priority Applications (no., kind, date): GB 19858713 A 19850403

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
GB 2173337	A	EN	22	18	
EP 197743	A	EN			

Regional Designated States,Original: DE FR IT

Alerting Abstract GB A

A ferroelectric liquid crystal layer whose pixels defined by the areas of overlap between the members of a first set of electrodes on one side of the liquid crystal layer and the members of a second set on the other side of the **layer** . The cell is **addressed** on a line-by-line basis by applying strobe pulses serially to the members of the first set while data pulses are applied in parallel to the members of the second set.

The strobe and data pulse waveforms are balanced bipolar pulses. In the addressing of any given pixel, by the co-operative action of a strobe pulse of a data pulse waveform includes a zero voltage step during at least a part of the strobe pulse.

ADVANTAGE - Achieves shorter line address time by modifying data, strobe pulse waveforms. **Switching** of cells may be made easier by incorporating zero-voltage steps in either or both of the data, strobe waveforms.

Equivalent Alerting Abstract US A

A cell is addressed on a line-by-line basis by applying pulses serially to the members of the first set of electrodes while data pulses are applied in parallel to the members of the second set. The strode and data pulse waveforms are balanced bipolar pulses, and the addressing of any given pixel by the co-operative action of a strobe pulse of a data pulse waveform includes a zero voltage step during at least a part of the strobe pulse.

Data entry is preceded with blanding (erasing) pulses applied to the strobe lines. The polarity of the stobing and blanking pulses is periodically reversed to maintain charge balance over a period.

USE/ADVANTAGE - For addressing **matrix arrays** of ferroelectric liquid crystall cells. Reduces min. line address time for giving address voltage, greater tolerance of reverse polarity voltages. (21pp)t

Title Terms/Index Terms/Additional Words: ADDRESS; **MATRIX** ; **ARRAY** ; FERROELECTRIC; LIQUID; CRYSTAL; CELL; PARALLEL; ENTER; BALANCE; BIPOLAR; DATA; PULSE; ONE; SET; ELECTRODE; COOPERATE; STROBE

Class Codes
International Classification (Main): **G06F-003/14**
(Additional/Secondary): G09F-009/35, G09G-003/36
US Classification, Issued: 340805000, 340784000, 359056000

File Segment: EngPI; EPI;
DWPI Class: T04; P85
Manual Codes (EPI/S-X): T04-H03B

25/5/9 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0002016504
WPI ACC NO: 1980-E8259C/
Electro-optically matrix **-addressed display with memory - has conductor rows and optical devices with input applied electric field and optical devices to** switch **electroluminescent layer**
Patent Assignee: IBM CORP (IBMC)
Inventor: ALT P M; SAHNI O
Patent Family (5 patents, 5 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
EP 11108	A	19800528	EP 1979103619	A	19790924	198022 B
US 4221002	A	19800902	US 1978958228	A	19781106	198038 E
CA 1127333	A	19820706				198230 E
EP 11108	B	19830921	EP 1979103619	A	19790924	198339 E
DE 2966192	G	19831027				198344 E

Priority Applications (no., kind, date): EP 1979103619 A 19790924; US 1978958228 A 19781106

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
EP 11108	A	EN			
Regional Designated States,Original: DE FR GB					
CA 1127333	A	EN			
EP 11108	B	EN			
Regional Designated States,Original: DE FR GB					

Alerting Abstract EP A
The display device comprises an electroluminescent layer with hysteresis in its luminance output versus voltage input characteristic having at least an on-state and an off-state. A number of rows of conductors apply locally an input electric field which alone is insufficient for **switching** the electroluminescent **layer** at the **location** to the on-state.
Optical devices apply an input illumination at the location which alone is insufficient for **switching** the electroluminescent **layer** at the **location** to the on-state. The illumination is sufficient with the applied input electric field to **switch** the electroluminescent layer to the on-state from the off state.

Title Terms/Index Terms/Additional Words: ELECTRO; OPTICAL; **MATRIX** ; ADDRESS; DISPLAY; MEMORY; CONDUCTOR; ROW; DEVICE; INPUT; APPLY; ELECTRIC; FIELD; **SWITCH** ; ELECTROLUMINESCENT; LAYER
Class Codes
International Classification (Main): **G06F-003/14**
(Additional/Secondary): **G06F-003/147** , G09F-013/22, G09G-003/12, G11C-011/42, G11C-013/04
US Classification, Issued: 365111000, 365110000, 365189090, 365231000, 365234000

File Segment: EngPI; EPI;
DWPI Class: T01; U14; P85
Manual Codes (EPI/S-X): T01-C04X; U14-J

36/5/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0007525960 - Drawing available
WPI ACC NO: 1996-139142/199614
XRPX Acc No: N1996-116584
High-speed low-power CMOS positive-shifted ECL I/O transmitter - includes first termination resistance having one terminal connected to first output terminal of output driver circuit
Patent Assignee: VLSI TECHNOLOGY INC (VLSI-N)
Inventor: DES ROSIERS A; DES ROSIERS A P; TA P D
Patent Family (2 patents, 19 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
US 5495184	A	19960227	US 1995371724	A	19950112	199614	B
WO 1996021972	A1	19960718	WO 1996US795	A	19960111	199634	E

Priority Applications (no., kind, date): US 1995371724 A 19950112

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 5495184	A	EN	13	5	
WO 1996021972	A1	EN	31	5	

National Designated States,Original: JP KR
Regional Designated States,Original: AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE

Alerting Abstract US A
An output driver circuit, comprising a first termination resistance RT1 which has one terminal connected to a first output terminal of the output driver circuit and which has the other terminal connected to a termination voltage source VT;
a first PMOS switch transistor M1, having a drain terminal, a source terminal, and a gate terminal, where the source terminal is connected to a VDD voltage source; a first switch device for providing a first switching signal to the gate terminal of the first PMOS switch transistor M1 for turning on and off current flow from the VDD voltage source through the first PMOS **switch** transistor M1; a **second** PMOS current-source transistor M2, having a drain terminal, a source terminal, and a gate terminal, where the source terminal of the second PMOS current-source transistor M2 is connected to the drain terminal of the first PMOS switch transistor M1 and where the source terminal of the second PMOS current-source transistor M2 is connected to the first output terminal of the output driver circuit.
A first DC voltage reference source REF A has an output terminal connected to the **gate** terminal of the **second** PMOS current-source transistor M2 for controlling the amount of current provided by the second PMOS current-source transistor M2 to the first termination resistance RT1; a first NMOS current-sink transistor M3, having a drain terminal, a source terminal, and a gate terminal, where the drain terminal is connected to the drain terminal of the second PMOS current-source transistor M2 and to the first output terminal of the output driver circuit; a second DC voltage reference source REF B having an output terminal connected to the gate terminal of the first NMOS current-sink transistor M3 for controlling the amount of current provided from the first termination resistance RT1 to the first NMOS current-sink transistor M3; a **second** NMOS **switch** transistor M4, having a drain terminal, a source terminal, and a gate terminal, the source terminal being connected to a VSS voltage source, where the drain terminal of the **second** NMOS **switch** transistor M4 is connected to the

source terminal of the first NMOS current-sink transistor M3 and where the source terminal of the **second** NMOS **switch** transistor N4 is connected to the VSS voltage source; and a **second switch** device for providing a **second switching signal** to the **gate** terminal of the **second** NMOS **switch** transistor M4 for turning off and on current flow to the VSS voltage source through the **second** NMOS **switch** transistor M4.

USE/ADVANTAGE - Efficient high-speed CMOS to ECL line driver capable of being fully integrated on a single chip.

Title Terms/Index Terms/Additional Words: HIGH; SPEED; LOW; POWER; CMOS; POSITIVE; SHIFT; ECL; TRANSMIT; FIRST; TERMINATE; RESISTANCE; ONE; TERMINAL; CONNECT; OUTPUT; DRIVE; CIRCUIT

Class Codes

International Classification (Main): H03K-019/0185
(Additional/Secondary): H03K-019/003
US Classification, Issued: 326073000, 326033000, 326083000, 327541000

File Segment: EPI;
DWPI Class: U21
Manual Codes (EPI/S-X): U21-C01B3; U21-C02A

17/5/11 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0006440211 - Drawing available
WPI ACC NO: 1993-243457/199330
Related WPI Acc No: 1997-448910; 1999-167620
XRPX Acc No: N1993-187270
Electrically erasable programmable read only memory - utilises source-side injection allowing very small programming currents
Patent Assignee: SANDISK CORP (SAND-N); SUNDISK CORP (SUND-N)
Inventor: FONG Y K; GUTERMAN D C; HARARI E; HARRAI E; SAMACHISA G
Patent Family (8 patents, 18 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
WO 1993014521	A1	19930722	WO 1993US265	A	19930112	199330	B
US 5313421	A	19940517	US 1992820364	A	19920114	199419	E
JP 8500937	W	19960130	JP 1993512628	A	19930112	199642	E
			WO 1993US265	A	19930112		
US 5776810	A	19980707	US 1992820364	A	19920114	199834	E
			US 1994193707	A	19940209		
US 5847996	A	19981208	US 1992820364	A	19920114	199905	E
			US 1994193707	A	19940209		
			US 1996639128	A	19960426		
US 5910915	A	19990608	US 1992820364	A	19920114	199930	E
			US 1994193707	A	19940209		
			US 1996639128	A	19960426		
			US 199865512	A	19980423		
US 5910925	A	19990608	US 1992820364	A	19920114	199930	E
			US 1994193707	A	19940209		
			US 1996639128	A	19960426		
			US 199865409	A	19980423		
JP 3738030	B2	20060125	JP 1993512628	A	19930112	200608	E
			WO 1993US265	A	19930112		

Priority Applications (no., kind, date): US 199865512 A 19980423; US 199865409 A 19980423; US 1996639128 A 19960426; US 1994193707 A 19940209; US 1992820364 A 19920114

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
WO 1993014521	A1	EN	51	8	
National Designated States,Original: JP					
Regional Designated States,Original: AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE					
US 5313421	A	EN	24	8	
JP 8500937	W	JA	69		PCT Application WO 1993US265 Based on OPI patent WO 1993014521
US 5776810	A	EN			Division of application US 1992820364 Division of patent US 5313421
US 5847996	A	EN			Continuation of application US 1992820364 Continuation of application US 1994193707 Continuation of patent US 5313421
US 5910915	A	EN			Division of application US 1992820364 Continuation of application US 1994193707 Division of application US 1996639128

US 5910925	A	EN		Division of patent US 5313421 Continuation of patent US 5776810 Division of application US 1992820364 Continuation of application US 1994193707 Division of application US 1996639128
JP 3738030	B2	JA	20	Division of patent US 5313421 Continuation of patent US 5776810 PCT Application WO 1993US265 Previously issued patent JP 08500937 Based on OPI patent WO 1993014521

Alerting Abstract WO A1

The memory structure (101 includes source (102) and drain (103) regions of a first conductivity type. A first channel region (106-1) of a second conductivity type is adjacent the source region. A second channel region (106-2) of the second conductivity type is between the drain region (103) and first channel region (106-1).

A floating gate (107) is above the second channel region (106-2). A first control gate (108) above the floating gate acts as a steering element for the memory transistor. A **second** control **gate** above the first channel region (106-1) acts as a control gate of an access transistor. A tunnelling zone is formed between the floating **gate** (107) and the **second** control **gate** .

ADVANTAGE - Utilizes very low programming currents, low programming voltage requirement, eliminating need for high voltage, immunity of programmability to increased levels of erase, adjustability of memory state for optimum read of both program and erased states and exhibits less susceptibility to source side hot electron programming induced trapping by establishing a separate threshold control at the region, facilitates multi-state cell sensing and exhibits potential for pure LV word line/decoder implementation.

Equivalent Alerting Abstract US A

Novel memory cells utilize source-side injection, allowing very small programming currents. If desired, to-be-programmed cells are programmed simultaneously while not requiring an unacceptably large programming current for any given programming operation. Pref., memory **arrays** are organized in sectors with each sector being formed of a single column or a group of columns having their control **gates** **connected** in common.

A high speed shift register is used in place of a row decoder to serially shift in data for the word lines, with all data for each word line of a sector being contained in the shift register on completion of its serial loading. In one embodiment, speed is improved by utilizing a parallel loaded buffer register which receives parallel data from the high speed shift register and holds that data during the write operation, allowing the shift register to receive serial loaded data during the write operation for use in a subsequent write operation.

ADVANTAGE - Source-side injection allows programming using very small programming currents.

Title Terms/Index Terms/Additional Words: ELECTRIC; ERASE; PROGRAM; READ; MEMORY; UTILISE; SOURCE; SIDE; INJECTION; ALLOW; CURRENT

Class Codes

International Classification (Main): G11C-013/00, H01L-021/336,

H01L-021/8247, H01L-029/68, H01L-029/78
(Additional/Secondary): G11C-016/02, G11C-016/04, G11C-016/06, H01L-027/115, H01L-029/788, H01L-029/792
International Classification (+ Attributes)
IPC + Level Value Position Status Version
G11C-0016/04 A I L B 20060101
H01L-0021/8247 A I F B 20060101
H01L-0027/115 A I L B 20060101
H01L-0029/788 A I L B 20060101
H01L-0029/792 A I L B 20060101
H01L-0021/70 C I F B 20060101
H01L-0029/66 C I L B 20060101
US Classification, Issued: 365185000, 365182000, 365184000, 365218000, 438258000, 438262000, 438264000, 438267000, 365185280, 365185260, 365185010, 365185280, 365185220, 365185140, 365185010, 365230010, 365189010

File Segment: EPI;
DWPI Class: U12; U13; U14
Manual Codes (EPI/S-X): U12-D02A1; U12-Q; U13-C04B2; U13-D02; U14-A03B7; U14-A07

30/5/21 (Item 19 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0004458154
WPI ACC NO: 1988-199646/
NAND stack read only memory array **- has adjacent columns tied to alternating sense amplifiers utilising multiplexer connected to virtual ground lines**
Patent Assignee: GEN INSTR CORP (GENN); MICROCHIP TECH INC (MICR-N)
Inventor: CLIADAKIS S H; HERDT C E
Patent Family (5 patents, 11 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
EP 275212	A	19880720	EP 1988300339	A	19880115	198829 B
US 4980861	A	19901225	US 19873837	A	19870116	199103 E
			US 1988287570	A	19881216	
IL 85117	A	19910730				199133 E
EP 275212	B1	19930804	EP 1988300339	A	19880115	199331 E
DE 3882720	G	19930909	DE 3882720	A	19880115	199337 E
			EP 1988300339	A	19880115	

Priority Applications (no., kind, date): US 1988287570 A 19881216; US 19873837 A 19870116
Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
EP 275212	A	EN	9	4	
Regional Designated States,Original: BE CH DE FR GB IT LI NL SE					
IL 85117	A	EN			
EP 275212	B1	EN	11	4	
Regional Designated States,Original: BE CH DE FR GB IT LI NL SE					
DE 3882720	G	DE			Application EP 1988300339
					Based on OPI patent EP 275212

Alerting Abstract EP A
The **array** is formed in a semiconductor substrate. The **array** comprises bit selectors and a number of bit switches each having an input and an output circuit. Each of the input circuits is connected to the bit selector. The output circuits are connected in series between two nodes to form a stack. Colinearly aligned stacks form a **column** . A **virtual** ground signal is applied to the first node. The signal applying device comprises a conductive region extending through the substrate in the direction of the column. The state of the second node is sensed pref. The second node is precharged to optimise the speed of the **array** .

A single stack select switch has an output circuit between the series connected output circuits of the bit switches and the second node. The stack select switch comprises an enhancement mode transistor. A multiplexer interposed between the sensor and the second node, or is connected to the conductive region.

ADVANTAGE - Faster access time by eliminating depletion mode decode transistors, thus reducing column capacitance. Horizontal ground straps of diffusion are eliminated to reduce chip area by running virtual ground lines vertically through **array** .

Equivalent Alerting Abstract US A
The NAND stack ROM **array** formed in a substrate has two parallel, spaced columns of series connected bit switching circuit formed in the substrate. Each of the circuit columns have a stack of the bit switching circuit. A first node at one end of the stack, a second node at the other end of the stack and stack decoder are provided. The stack decoder has a single

enhancement mode transistor interposed between the stack and the first node. A circuit precharges the first node and first and second sense amplifiers. The first node of a selected column are connected with one of sense amplifiers.

to connecting wire associated with selected columns to actuate them and to the second node of the selected columns. The signal applying circuit has a conductive region extending between and in the same general direction in the substrate as the columns.

ADVANTAGE - Faster access time. @(8pp)@

Title Terms/Index Terms/Additional Words: NAND; STACK; READ; MEMORY; **ARRAY**; ADJACENT; COLUMN; TIE; ALTERNATE; SENSE; AMPLIFY; UTILISE; MULTIPLEX; CONNECT; VIRTUAL; GROUND; LINE; ROM

Class Codes

International Classification (Main): G11C-017/00
(Additional/Secondary): G11C-007/00
US Classification, Issued: 365203000, 365104000

File Segment: EPI;
DWPI Class: U13; U14
Manual Codes (EPI/S-X): U13-C04A; U14-A06B5

File 348:EUROPEAN PATENTS 1978-2006/ 200638
(c) 2006 European Patent Office
File 349:PCT FULLTEXT 1979-2006/UB=20060928UT=20060921
(c) 2006 WIPO/Thomson

Set	Items	Description
S1	864158	MATRIX OR MATRICES OR ARRAY? ? OR TABLE? ? OR ROW? ?(3N)COLUMN? ?
S2	1512826	ADDRESS???? OR POINTER? ? OR REFERENCE? ? OR LOCATION? ? OR LOCATOR? ?
S3	891258	LAYER??? OR SUBLAYER??? OR MULTILAYER? ? OR BAND? ? OR STRATUM OR STRATA
S4	488636	SWITCH??? OR GATE OR GATES
S5	106260	S4(3N)(CONNECT???? OR LINK??? OR CHAIN??? OR ATTACH?????)
S6	623363	SERIAL? OR SEQUENTIAL? OR SUCCESSIVE?
S7	482	VIRTUAL??(3N)COLUMN? ?
S8	113262	S4(3N)(TWO OR SECOND OR 2ND OR DUAL OR TWIN OR COUPLE OR ANOTHER OR ADDITIONAL OR DIFFERENT)
S9	8569	S1(20N)S2(3N)S3
S10	154	S9(100N)S5
S11	1	S10(100N)S7
S12	45	S10(100N)S8
S13	35	S12 NOT AD=20000817:20030817/PR
S14	34	S13 NOT AD=20030817:20061003/PR
S15	34	IDPAT (sorted in duplicate/non-duplicate order)
S16	33	IDPAT (primary/non-duplicate records only)
S17	4	S9(100N)S7
S18	32	S1(50N)S2(50N)S3(100N)S7
S19	28	S18 NOT (S12 OR S17)
S20	22	S19 NOT AD=20000817:20030817/PR
S21	20	S20 NOT AD=20030817:20061003/PR

16/3,K/9 (Item 9 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00999083
Microcomputer with flash memory programmable via external terminal
Mikrorechner mit uber eine aussere Anschlussklemme programmierbarem Flashspeicher
Micro-ordinateur comprenant une memoire flash programmable au moyen d'une borne externe
PATENT ASSIGNEE:
Hitachi, Ltd., (204145), 6 Kanda Surugadai 4-chome, Chiyoda-ku, Tokyo 101-8010, (JP), (Proprietor designated states: all)
HITACHI ULSI ENGINEERING CORP., (1773080), 20-1, Josuihoncho 5-chome, Kodaira-shi, Tokyo, (JP), (Proprietor designated states: all)
INVENTOR:
Matsubara, Kiyoshi, 20-6, Takeoka-3-chome,, Kiyose-shi, Tokyo, (JP)
Yashiki, Naoki, 17-10, Josuishinmachi-1-chome, Kodaira-shi, (JP)
Baba, Shiro, 9-17, Tokura-4-chome, Kokubunji-shi, (JP)
Ito, Takashi, 15-9, Higashikoigakubo-4-chome, Kokubunji-shi, (JP)
Mukai, Hirofumi, 20-12, Sakai-1-chome, Musashino-shi, (JP)
Sato, Masanao, 103, 11-14, Matsubara-2-chome, Setagaya-ku, Tokyo, (JP)
Terasawa, Masaaki, 32-9, Nakagamicho-2-chome, Akishima-shi, (JP)
Kuroda, Kenichi, 29-28, Sunagawacho-6-chome, Tachikawa-shi, (JP)
Shiba, Kazuyoshi, 301, 32-13, Ogawahigashicho-1-chome,, Kodaira-shi, (JP)
LEGAL REPRESENTATIVE:
Strehl Schubel-Hopf & Partner (100941), Maximilianstrasse 54, 80538 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 902436 A2 990317 (Basic)
EP 902436 A3 990519
EP 902436 B1 021016
APPLICATION (CC, No, Date): EP 98118739 930311;
PRIORITY (CC, No, Date): JP 9291919 920317; JP 9293908 920319
DESIGNATED STATES: DE; FR; GB; IT
RELATED PARENT NUMBER(S) - PN (AN):
EP 561271 (EP 93103907)
RELATED DIVISIONAL NUMBER(S) - PN (AN):
EP 1094470 (EP 2000121759)
INTERNATIONAL PATENT CLASS (V7): G11C-016/06; G06F-009/445
ABSTRACT WORD COUNT: 107
NOTE:
Figure number on first page: 1

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	199911	1542
CLAIMS B	(English)	200242	1069
SPEC A	(English)	199911	29262
SPEC B	(English)	200242	29453
Total word count - document A			30809
Total word count - document B			30522
Total word count - documents A + B			61331

...SPECIFICATION a memory array in which memory cells formed of insulated gate field effect transistors of **two - layer gate** structure explained in **connection** with Figs 11A and 11B are arranged in **matrix** . In this memory **array** ARY, like the construction explained with **reference** to Fig. 13, control gates of memory cells are connected to a corresponding word line...in the figure is incorporated in a microcomputer. In the

figure, 210 designates a memory **array** in which memory cells each constructed of an insulated gate field effect transistor of **two - layer gate** structure as previously explained with **reference** to, for example, Fig. 11 are arranged in **matrix** . In the memory **array** ARY, as in the case of the configuration explained in connection with Fig. 25, memory cells have control **gates connected** to corresponding word lines, drain regions connected to corresponding data lines and source regions connected...

...SPECIFICATION a memory array in which memory cells formed of insulated gate field effect transistors of **two - layer gate** structure explained in **connection** with Figs 11A and 11B are arranged in **matrix** . In this memory **array** ARY, like the construction explained with **reference** to Fig. 13, control gates of memory cells are connected to a corresponding word line...in the figure is incorporated in a microcomputer. In the figure, 210 designates a memory **array** in which memory cells each constructed of an insulated gate field effect transistor of **two - layer gate** structure as previously explained with **reference** to, for example, Fig. 11 are arranged in **matrix** . In the memory **array** ARY, as in the case of the configuration explained in connection with Fig. 25, memory cells have control **gates connected** to corresponding word lines, drain regions connected to corresponding data lines and source regions connected...

21/3,K/10 (Item 10 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00565979
Electro-optical plasma addressing device
Plasmaadressierte elektrooptische Vorrichtung
Dispositif electro-optique adresse a plasma
PATENT ASSIGNEE:
SONY CORPORATION, (214022), 7-35, Kitashinagawa 6-chome Shinagawa-ku, Tokyo, (JP), (applicant designated states: DE;FR;GB)
INVENTOR:
Hayashi, Masatake, c/o Sony Corporation, 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo, (JP)
Nishida, Motoharu, c/o Sony Corporation, 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo, (JP)
LEGAL REPRESENTATIVE:
Muller, Frithjof E., Dipl.-Ing. (8661), Patentanwalte MULLER & HOFFMANN, Innere Wiener Strasse 17, 81667 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 567019 A1 931027 (Basic)
EP 567019 B1 970910
APPLICATION (CC, No, Date): EP 93106245 930416;
PRIORITY (CC, No, Date): JP 92128265 920421
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS (V7): G02F-001/133;
ABSTRACT WORD COUNT: 184

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	9709W1	422
CLAIMS B	(German)	9709W1	404
CLAIMS B	(French)	9709W1	457
SPEC B	(English)	9709W1	3575
Total word count - document A			0
Total word count - document B			4858
Total word count - documents A + B			4858

...SPECIFICATION Invention
The present invention relates to an electro-optical plasma addressing device having a two- **layer** construction, consisting of an electro-optical cell, such as a liquid crystal cell, and a...

...the picture elements and drives the switching elements in linear sequence. Since the active matrix **addressing** system needs a substrate provided with a plurality of semiconductor elements, such as thin-film...
...instead of the switching elements, such as thin-film transistors. The construction of a plasma **addressing** display employing plasma switches for driving a liquid crystal cell will be briefly described hereinafter.
Referring to Fig. 6, the plasma **addressing** display has a laminate flat panel construction comprising a liquid crystal cell 101, a plasma...

...with a plurality of parallel grooves 105 extending, for example, along the rows of a **matrix** . The grooves 105 are covered closely with the middle plate 103 to form separate plasma...

...electrodes D extend perpendicularly to the axes of the plasma chambers 106 to function as **column** driving units. The **virtual** intersections of the row scanning units and the column driving units form a **matrix** of picture elements.

The operation of the plasma **addressing** display of Fig. 6 will be described briefly with **reference** to Fig. 7.

An external driving circuit for driving the plasma **addressing** display comprises a signal circuit 201, a scanning circuit 202 and a control circuit 203...for the corresponding discharge portions s. Thus, the display panel of the electro-optical plasma **addressing** device is provided internally with loading resistors instead of external resistors, which are needed by the discharge electrodes of the conventional plasma **addressing** device, and the loading resistors can be easily incorporated into the second electrodes by forming...

...cathode K, forms one row scanning unit. The first electrodes D extending perpendicularly to the **row** scanning units form **column** driving units. The **virtual** intersections of the row scanning units and the column driving units formed at right angles define picture elements in the liquid crystal **layer** 6. As shown in Fig. 2, three pairs of discharge portions s are allocated to...

16/3,K/11 (Item 11 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00966517
Semiconductor memory device
Halbleiterspeicheranordnung
Dispositif de memoire a semiconducteurs
PATENT ASSIGNEE:
MITSUBISHI DENKI KABUSHIKI KAISHA, (208581), 2-3, Marunouchi 2-chome Chiyoda-ku, Tokyo, (JP), (Proprietor designated states: all)
MITSUBISHI ELECTRIC ENGINEERING CO., LTD., (1515570), 6-2 Ohte-machi 2-chome, Chiyoda-ku, Tokyo, (JP), (Proprietor designated states: all)
INVENTOR:
Dosaka, Katsumi, c/o Mitsubishi Denki K.K., LSI Kenkyusho, Mizuhara 4-chome, Itami-shi, Hyogo-ken, (JP)
Kumanoya, Masaki, c/o Mitsubishi Denki K.K., LSI Kenkyusho, Mizuhara 4-chome, Itami-shi, Hyogo-ken, (JP)
Yamazaki, Akira, c/o Mitsubishi Denki K.K., LSI Kenkyusho, Mizuhara 4-chome, Itami-shi, Hyogo-ken, (JP)
Iwamoto, Hisashi, c/o Mitsubishi Denki K.K., LSI Kenkyusho, Mizuhara 4-chome, Itami-shi, Hyogo-ken, (JP)
Konishi, Yasuhiro, c/o Mitsubishi Denki K.K., LSI Kenkyusho, Mizuhara 4-chome, Itami-shi, Hyogo-ken, (JP)
Hayano, Kouji, c/o Mitsubishi Denki K.K., Kitaitami Seisakusho, 1 Mizuhara 4-chome, Itami-shi, Hyogo-ken, (JP)
Abe, Hideaki, c/o Mitsubishi Denki K.K., Kitaitami Seisakusho, 1 Mizuhara 4-chome, Itami-shi, Hyogo-ken, (JP)
Himukashi, Katsumitsu, c/o Mitsubishi E. E. Co.Ltd, LSI Eng. Off., 61-5 Higashino 4-chome, Itami-shi, Hyogo-ken, (JP)
Ishizuka, Yasuhiro, c/o Mitsubishi E. E. Co. Ltd, LSI Eng. Off., 61-5 Higashino 4-chome, Itami-shi, Hyogo-ken, (JP)
Saiki, Tsukasa, c/o Mitsubishi Elec. Eng. Co. Ltd., LSI Eng. Off., 61-5 Higashino 4-chome, Itami-shi, Hyogo-ken, (JP)
LEGAL REPRESENTATIVE:
Beresford, Keith Denis Lewis et al (28273), BERESFORD & Co. 2-5 Warwick Court, High Holborn, London WC1R 5DH, (GB)
PATENT (CC, No, Kind, Date): EP 877384 A2 981111 (Basic)
EP 877384 A3 990825
EP 877384 B1 020116
APPLICATION (CC, No, Date): EP 98201559 920416;
PRIORITY (CC, No, Date): JP 9185625 910418; JP 91212140 910823; JP 91242286 910924; JP 9217809 920203
DESIGNATED STATES: DE; FR; GB; IT
RELATED PARENT NUMBER(S) - PN (AN):
EP 509811 (EP 92303424)
INTERNATIONAL PATENT CLASS (V7): G11C-011/00; G11C-011/418; G11C-011/419
ABSTRACT WORD COUNT: 230
NOTE:
Figure number on first page: 9

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	199846	4598
CLAIMS B	(English)	200203	4194
CLAIMS B	(German)	200203	3774
CLAIMS B	(French)	200203	5316
SPEC A	(English)	199846	90305
SPEC B	(English)	200203	86300
Total word count - document A			94917

Total word count - document B 99584
Total word count - documents A + B 194501

...SPECIFICATION and SW2 and a ground line GND are arranged in parallel and formed by a **second** layer aluminum interconnection (second aluminum interconnection). Bit lines SBL1, *SBL1, SBL2 and *SBL2 are formed... drain connected to bit line SBL1 through a contact hole CX1, its gate and source **connected** to the first layer aluminum interconnection through contact holes CX3 and CX2, and this first...

...SBL1 formed of the first layer aluminum interconnection through a contact hole CX5, and its **gate** and source **connected** to the first layer aluminum interconnection layer through contact holes CX4 and CX2, and this...

...line Vcc through contact hole CX6.
Transistor SQ1 has its drain connected to the first **layer** aluminum interconnection through a contact hole CX8, and this first layer aluminum interconnection is connected...

...fourth layer polysilicon interconnection connected to contact hole CX9 provides node SN1. Node SN1 is **connected** to **gate** electrodes of transistors SQ2 and SQ4 through the fourth layer polysilicon interconnection and contact hole...

...to one conduction terminal of transistor SQ5 through contact hole CX16.
Transistor SQ1 has its **gate** **connected** to node SN2 through contact hole CX10 and through the fourth layer polysilicon interconnection. Transistor...

...SPECIFICATION SQ7 has its drain connected to bit line SBL1 through a contact hole CX1, its **gate** and source **connected** to the first layer aluminum interconnection through contact holes CX3 and CX2, and this first...

...SBL1 formed of the first layer aluminum interconnection through a contact hole CX5, and its **gate** and source **connected** to the first layer aluminum interconnection layer through contact holes CX4 and CX2, and this...

...line Vcc through contact hole CX6.
Transistor SQ1 has its drain connected to the first **layer** aluminum interconnection through a contact hole CX8, and ...fourth layer polysilicon interconnection connected to contact hole CX9 provides node SN1. Node SN1 is **connected** to **gate** electrodes of transistors SQ2 and SQ4 through the fourth layer polysilicon interconnection and contact hole ...

...to one conduction terminal of transistor SQ5 through contact hole CX16.
Transistor SQ1 has its **gate** **connected** to node SN2 through contact hole CX10 and through the fourth layer polysilicon interconnection. Transistor...

16/3,K/20 (Item 20 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00477573
Active matrix liquid crystal display devices.
Flussigkristall-Anzeigevorrichtungen mit aktiver Matrix.
Dispositifs d'affichage a cristal liquide a matrice active.
PATENT ASSIGNEE:
PHILIPS ELECTRONICS UK LIMITED, (215201), Philips House 1-19 Torrington Place, London WC1E 7HD, (GB), (applicant designated states: GB)
N.V. Philips' Gloeilampenfabrieken, (200769), Groenewoudseweg 1, NL-5621 BA Eindhoven, (NL), (applicant designated states: DE;FR)
INVENTOR:
Shannon, John Martin, c/o Philips Research Laboratories, Redhill, Surrey RH1 5HA, (GB)
LEGAL REPRESENTATIVE:
Williamson, Paul Lewis et al (37771), PHILIPS ELECTRONICS Patents and Trade Marks Department Philips House 188 Tottenham Court Road, London W1P 9LE, (GB)
PATENT (CC, No, Kind, Date): EP 464897 A2 920108 (Basic)
EP 464897 A3 920812
APPLICATION (CC, No, Date): EP 91201557 910619;
PRIORITY (CC, No, Date): GB 9014257 900627
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS (V7): G02F-001/136;
ABSTRACT WORD COUNT: 146

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	337
SPEC A	(English)	EPABF1	3983
Total word count - document A			4320
Total word count - document B			0
Total word count - documents A + B			4320

...SPECIFICATION provide an improved active matrix liquid crystal display device using metal light shields for the **switching** devices.
It is **another** object of the present invention to provide light shields for the switching devices of an...

...which is connected electrically to a row address conductor adjacent the one to which the **switching** device is **connected** . Although the interconnection between the light shield at the region of the switching device and...
...row address conductor.
The invention derives from the recognition that if a metallic light screening **layer** is contacted to an adjacent row address conductor the increase in capacitive cross-talk can be negligible. In operation, each row **address** conductor is at predetermined potential for most of the time. In conventional TFT **matrix addressed** display devices the drive circuit applies to the row **address** conductors a constant **reference** potential, for example ground potential, except during the comparatively very short period when a gating...

21/3,K/19 (Item 5 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00281664
ADDRESSING METHOD AND SYSTEM HAVING MINIMAL CROSSTALK EFFECTS
PROCEDE ET SYSTEME D'ADRESSAGE REDUISANT AU MINIMUM LES EFFETS D'INTERFERENCE
Patent Applicant/Assignee:
IN FOCUS SYSTEMS INC,
MOTOROLA INC,
Inventor(s):
PRINCE Dennis W,
GROSSPIETSCH John K,
CLIFTON Benjamin Robert,
SCHEFFER Terry J,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9429842 A1 19941222
Application: WO 94US6529 19940610 (PCT/WO US9406529)
Priority Application: US 9377859 19930616
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AU CA JP KR AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Fulltext Word Count: 12172

Fulltext Availability:
Detailed Description

Detailed Description
... primarily from differences in column signals caused by different images being displayed. In the Active **Addressing** .. technique,, however,, the rows generally have different row signals. For example, the Active Addressing" technique...

...that the majority of spectral components of the pixel voltage waveforms appear within a frequency **band** in which the optical response of the display is relatively independent of frequency.

One method...

...a frame period but increases the frequency of their components. In a preferred embodiment, the **row** and **column** signals are modulated by a Manchester pulse using circuitry that reverses the polarity of the **row** and **column** signals for part of an addressing interval. Many other modulation schemes can be used to...

...each pixel by defining virtual pixels. Virtual pixels are defined by the intersection of the **column** electrodes with a **virtual** row electrode and each virtual pixel has an associated virtual information elements. The values of...adjusting the amplitude of frequency components that lie outside of the constant optical response

frequency **band** .

Another adaptive method of modifying the column addressing signals typically entails determining the spectral components of the column voltage waveform and adjusting the amplitude of the column **addressing** signal to compensate for the sensitivity of the optical state transmission to those spectral components...

...waveform is found to include significant spectral components at low frequencies, the amplitude of the **row** or **column** signal is reduced to compensate for the increased transmission of the optical state at low...

...number of frequencies rather than analyzing-the entire spectrum. Adjusting the amplitude of the column **addressing** signals changes the amplitude of the frequency components in all frequency bands.

Row signals that...

...frequency band can also be adaptively or non-adaptively determined. For example, in the Active **Addressing** ' technique using row functions derived from Walsh functions, the column gradient induced by different sequencies...

...functions can be non adaptively modified by applying the modulation schemes described above. Alternatively, row **addressing** signals can also be adaptively adjusted in amplitude to compensate for the variation in frequency components of the row signals used in the Active **Addressing** ' technique. Both row and column **addressing** signals, and any combination thereof, can be determined using an adaptive, non-adaptive method, or...combined into the row signal generator 24 or column signal generator 20 to generate directly **addressing** signal that de-emphasize components outside of middle frequency band 54.

Walsh functions are typically...

...to Fig, 23o A virtual row 264 defines virtual pixels 266 by the overlap of **column** electrodes 11 and **virtual** row 264. With every real pixel 14, there is associated an information element 268 whose...display 2 and Ii is the value of pixel information elements 268 in the ith **row** 16 of the **column** ,
In Alt and Pleshko addressing using the virtual pixel gray level method, the column signal...

...where I'D" is the column voltage applied to a fully ON pixel 14. The **addressing** interval has a duration, &t, that equals the frame period, T, divided by the sum...

...virtual rows 264, n, thus, &t=T/(N+n).

In a system using an Active **Addressing** "' technique, the amplitude of the column signal during any

addressing interval is proportional to the sum of the products of the real or virtual information...

...and virtual pixels, 14 and 266 in the column 11. For purposes of determining the **column** signals, **virtual rows** 264 are considered to be **addressed** by an appropriate active **addressing** function. The signal for each column 18 during any **addressing** interval, equals.

$$\sum_{i=N+n}^{N} P_i V_{Jk}$$

where Pi is the amplitude of the row signal applied to that row 16 during the **addressing** interval, Vk is the value of the ith virtual information element 270, calculated as described...

...is the amplitude of the row signal associated with that virtual row 264 during the **addressing** interval.

In this equation, the normalized, or rms values, of the row signals are equal...

16/3,K/29 (Item 29 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00545277 **Image available**
MRAM ARRAY HAVING A PLURALITY OF MEMORY BANKS
GROUPEMENT DE MEMOIRES MAGNETIQUES RAM AVEC PLUSIEURS BLOCS MEMOIRE
Patent Applicant/Assignee:
MOTOROLA INC,
Inventor(s):
NAJI Peter K,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200008650 A1 20000217 (WO 0008650)
Application: WO 99US17581 19990803 (PCT/WO US9917581)
Priority Application: US 98128020 19980803
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
JP KP SG AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Fulltext Word Count: 4838

Fulltext Availability:
Claims
Claim
... memory cell has a
first magnetic layer, a second magnetic layer, and a non
magnetic **layer** sandwiched by the first and second magnetic
layers ,, the first magnetic **layer** electrically connected to
the first line.

10 The magnetic random access memory **array** as claimed
in claim 9 further including a plurality of **switches** , each
switch **connected** to each **second** line for electrically
coupling the second **layer** of each magnetic memory to a
common line.
/3
BIT/ **REFERENCE** LINE SELECTOR
58 58@ 58 58@
34 5 6
10- -1 10-- A 10- - lo...

```
File   2:INSPEC 1898-2006/Sep W4
         (c) 2006 Institution of Electrical Engineers
File   6:NTIS 1964-2006/Sep W4
         (c) 2006 NTIS, Intl Cpyrght All Rights Res
File   8:Ei Compendex(R) 1970-2006/Sep W4
         (c) 2006 Elsevier Eng.  Info. Inc.
File  20:Dialog Global Reporter 1997-2006/Oct 03
         (c) 2006 Dialog
File  23:CSA Technology Research Database 1963-2006/Sep
         (c) 2006 CSA.
File  34:SciSearch(R) Cited Ref Sci 1990-2006/Sep W4
         (c) 2006 The Thomson Corp
File  35:Dissertation Abs Online 1861-2006/Sep
         (c) 2006 ProQuest Info&Learning
File  65:Inside Conferences 1993-2006/Oct 03
         (c) 2006 BLDSC all rts. reserv.
File  94:JICST-EPlus 1985-2006/Jun W4
         (c)2006 Japan Science and Tech Corp(JST)
File  95:TEME-Technology & Management 1989-2006/Sep W4
         (c) 2006 FIZ TECHNIK
File  99:Wilson Appl. Sci & Tech Abs 1983-2006/Jul
         (c) 2006 The HW Wilson Co.
File 111:TGG Natl.Newspaper Index(SM) 1979-2006/Sep 19
         (c) 2006 The Gale Group
File 144:Pascal 1973-2006/Sep W2
         (c) 2006 INIST/CNRS
File 256:TecInfoSource 82-2006/Jan
         (c) 2006 Info.Sources Inc
File  56:Computer and Information Systems Abstracts 1966-2006/Sep
         (c) 2006 CSA.
File  57:Electronics & Communications Abstracts 1966-2006/Sep
         (c) 2006 CSA.
File  68:Solid State & Superconductivity Abstracts 1966-2006/Sep
         (c) 2006 CSA.
File  60:ANTE: Abstracts in New Tech & Engineer 1966-2006/Sep
         (c) 2006 CSA.
File 293:Engineered Materials Abstracts 1966-2006/Sep
         (c) 2006 CSA.
File 239:Mathsci 1940-2006/Nov
         (c) 2006 American Mathematical Society

Set     Items   Description
S1    5167769   MATRIX OR MATRICES OR ARRAY? ? OR TABLE? ? OR ROW? ?(3N)CO-
            LUMN? ?
S2    7295361   ADDRESS???? OR POINTER? ? OR REFERENCE? ? OR LOCATION? ? OR
             LOCATOR? ?
S3    5806077   LAYER??? OR SUBLAYER??? OR MULTILAYER? ? OR BAND? ? OR STR-
            ATUM OR STRATA
S4    2495574   SWITCH??? OR GATE OR GATES
S5      39548   S4(3N)(CONNECT???? OR LINK??? OR CHAIN??? OR ATTACH?????)
S6    1303086   SERIAL? OR SEQUENTIAL? OR SUCCESSIVE?
S7        381   VIRTUAL??(3N)COLUMN? ?
S8     109202   S4(3N)(TWO OR SECOND OR 2ND OR DUAL OR TWIN OR COUPLE OR A-
            NOTHER OR ADDITIONAL OR DIFFERENT)
S9       1356   S1 AND S2(3N)S3
S10        14   S9 AND S5
S11        12   RD  (unique items)
S12         9   S11 NOT PY=2001:2006
S13       232   S9 AND (MEMORY  OR RAM OR DRAM OR MRAM OR VRAM OR PROM OR -
            EPROM OR EEPROM OR SEMICONDUCTOR? ? OR CHIP? ? OR IC OR INTEG-
            RATED()CIRCUIT? ?)
```

```
S14          60   S13 AND S4
S15          48   RD  (unique items)
S16           6   S13 AND S8
S17           6   RD  (unique items)
S18          37   S15 NOT (S17 OR S11)
S19          16   S18 NOT PY=2001:2006
S20           0   S9 AND S7
S21          26   S1 AND S7
S22          22   RD  (unique items)
S23          13   S22 NOT PY=2001:2006
S24          13   S23 NOT (S17 OR S11 OR S18)
S25      149053   (TWO OR SECOND OR 2ND OR DUAL OR TWIN OR COUPLE OR ANOTHER
                  OR ADDITIONAL OR DIFFERENT)(3N)SIGNAL?
S26           7   S25 AND S9
S27           5   RD  (unique items)
```

19/5/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

05904884 INSPEC Abstract Number: B9504-0170J-028
Title: Performance enhancement of multilayer PBGA
Author(s): Duraiswami, N.; Huang, W.
Author Affiliation: Motorola Inc., Austin, TX, USA
p.118-23
Publisher: ISHM Microelectron. Soc, Reston, VA, USA
Publication Date: 1994 Country of Publication: USA xiv+648 pp.
ISBN: 0 930815 41 6
Conference Title: Proceedings of 27th International Symposium on Microelectronics
Conference Sponsor: Int. Soc. Hybrid Microelectron
Conference Date: 15-17 Nov. 1994 Conference Location: Boston, MA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: Plastic Ball Grid **Array** (PBGA) package is gaining momentum in higher performance applications because of its comparative smaller size and performance gain over peripherally-leaded structures. This paper **addresses** modeling of **multilayer** PBGAs with complicated current paths and reference planes. As PBGA design becomes more complicated, as with a four metal layer structure (two signal layers, one power and one ground layer), accurate performance estimation is necessary. For high performance **chips**, the package design becomes a performance design. This concept has been applied to our work. In this paper, we discuss design improvements for **switching** noise reduction to meet the ground bounce criteria of a FSRAM. Two design versions are discussed: initial design was reviewed and the modified design is suggested with better electrical performance. (5 Refs)
Subfile: B
Descriptors: BiCMOS **memory** circuits; **integrated circuit** modelling; **integrated circuit** technology; packaging; **semiconductor** device noise; SRAM **chips**
Identifiers: performance enhancement; multilayer PBGA; higher performance applications; BiCMOS SRAM
Class Codes: B0170J (Product packaging); B2570K (Mixed technology integrated circuits); B1265D (Memory circuits); B2570A (Integrated circuit modelling and process simulation)

19/5/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

04636686 INSPEC Abstract Number: B90035037, C90036884
Title: ORCA: a sea-of- gates **place and route system**
Author(s): Igusa, M.; Beardslee, M.; Sangiovanni-Vincentelli, A.
Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., California Univ., Berkeley, CA, USA
Conference Title: 26th ACM/IEEE Design Automation Conference (ACM No.477890 and IEEE Cat. No.89CH2734-2) p.122-7
Publisher: ACM, New York, NY, USA
Publication Date: 1989 Country of Publication: USA xxvi+839 pp.
ISBN: 0 89791 310 8
U.S. Copyright Clearance Center Code: 0-89791-310-8/89/0006-0122$01.50
Conference Sponsor: IEEE; ACM
Conference Date: 25-29 June 1989 Conference Location: Las Vegas, NV, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: A description is given of ORCA, a sea-of- **gates** place and route system, whose objective is to produce the highest density layout by fully exploiting the inherent features of this design style. The ORCA system starts with a module generator which preprocesses **memory arrays** and other logic with a regular structure to form high-density macros. The remaining logic is clustered together to form flexible macros, which are called porous. The porous macro-cells allow global routing to pass through the macro instead of detouring around its perimeter. The porous macros are dynamically shaped and resized by interaction with global wiring analysis. A general channelless area router has been developed to **address** the multiple **layers** of interconnect and routing areas which will be dominantly over-the-cell. Due to the large size of the problem (e.g., 100000 **gates**), the placement and routing algorithms are hierarchical. Test results are presented. (11 Refs)
Subfile: B C
Descriptors: circuit layout CAD; macros
Identifiers: high density layout; placement algorithms; **memory array** preprocessing; clustered logic; dynamic shaping; resizing; hierarchical algorithms; multiple interconnect layers; sea-of- **gates** place and route system; ORCA; module generator; high-density macros; flexible macros; porous macro-cells; global routing; global wiring analysis; channelless area router; routing algorithms
Class Codes: B1130B (Computer-aided circuit analysis and design); C7410D (Electronic engineering)

19/5/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

04577825 INSPEC Abstract Number: B90014123, C90020415
Title: A 23 ns 256 K EPROM with double- layer metal and address transition detection
Author(s): Hoff, D.; Pathak, S.; Payne, J.; Shrivastava, R.; Arreola, J.; Norris, C.; Tsao, S.-C.; Prickett, B.; Orput, M.
Author Affiliation: Cypress Semicond. Corp., San Jose, CA, USA
Conference Title: 1989 IEEE International Solid-State Circuits Conference. Digest of Technical Papers. 36th ISSCC. First Edition (Cat. No.CH2684-9) p.130-1, 312
Publisher: IEEE, New York, NY, USA
Publication Date: 1989 Country of Publication: USA 394 pp.
U.S. Copyright Clearance Center Code: 0193-6530/89/0000-0130$01.00
Conference Sponsor: IEEE; Univ. Pennsylvania
Conference Date: 15-17 Feb. 1989 Conference Location: New York, NY, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: A 256 K **EPROM** (electrically programmable read-only **memory**) is described in which 23-ns access time was achieved by a combination of advanced CMOS processing, double-layer metal (DLM), differential sensing, address transition detection (ATD), and a ground- **switched** decoding scheme. DLM is used to strap wordlines in the **array** and bus signals in the periphery. Performance is obtained by reducing bit line length to 256 cells, with 2048 cells per word line. This results in a 70.5-mil*229.8-mil **array** with an efficiency of 41.2%. Die size is 116 mil*339 mil. Short bit lines result in a total column and Y-select capacitance of 1.3 pF. Word line RC delay is only 0.8 ns. DLM saves 7.3 ns over an optimized silicide design using two word line drivers. The 0.8- mu m CMOS DLM **EPROM** technology yields a typical unloaded ring oscillator **gate** delay of 115 ps. Lightly doped drain (LLD) is used on both NMOS and PMOS devices for reliability and performance. Ti/Al metalization improves metal reliability. A composite interpoly dielectric is used for improved FAMOS (floating- **gate** avalanche-injection MOS) reliability. (2 Refs)
Subfile: B C
Descriptors: CMOS **integrated circuits** ; **EPROM** ; integrated **memory** circuits
Identifiers: FAMOS reliability improvement; lightly doped drain; **EPROM** ; double-layer metal; address transition detection; electrically programmable read-only **memory** ; access time; advanced CMOS processing; differential sensing; address transition detection; ground- **switched** decoding scheme; Y-select capacitance; metal reliability; composite interpoly dielectric; floating- **gate** avalanche-injection MOS; 41.2 percent; 1.3 pF; 0.8 micron; 23 ns; 256 kbit; Ti-Al metallisation
Class Codes: B1265D (Memory circuits); B2570D (CMOS integrated circuits); C5320G (Semiconductor storage)
Chemical Indexing:
Ti-Al int - Al int - Ti int - Al el - Ti el (Elements - 1,1,2)
Numerical Indexing: efficiency 4.12E+01 percent; capacitance 1.3E-12 F; size 8.0E-07 m; time 2.3E-08 s; storage capacity 2.62E+05 bit

24/5/2 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

1380933 NTIS Accession Number: AD-A193 521/2
Systolic Array **Fault Tolerance Performance Analysis** (Summary rept)
Choinski, T. C. ; Leonhardt, M. H.
Naval Underwater Systems Center, New London, CT. New London Lab.
Corp. Source Codes: 055030001; 405918
Report No.: NUSC-TR-8221
5 Apr 88 56p
Languages: English
Journal Announcement: GRAI8819
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A04/MF A01
Country of Publication: United States
The reliability performance of six different systolic **array** fault tolerance techniques are determined and compared in terms of mean time between failure (MTBF). The six techniques include redundant **arrays** , companion processors, sequential row elimination (SRE), alternate **row** and **column** elimination (ARCE), **virtual** **arrays** , and tree based architectures. The results demonstrate the importance of the switching function failure rate in achieving theoretical capability. Virtual **arrays** were found to have the best theoretical potential for improving the reliability of systolic **arrays** when high throughput is required. All techniques provided comparable performance for low throughput levels. The potential application of graceful degradation techniques to the minimum variance distortionless response (MVDR) adaptive beamforming algorithm is discussed.
Descriptors: *Adaptive systems; *Computer architecture; *Fault tolerant computing; Algorithms; **Arrays** ; Beam forming; Degradation; Distortion; Elimination; Failure; Functions; Redundancy; Reliability; Response; Switching; Variations
Identifiers: MTBF(Mean Time Between Failure); Sequential processing; Virtual memories; Performance evaluation; NTISDODXA
Section Headings: 62B (Computers, Control, and Information Theory--Computer Software)

24/5/9 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

06378667 Genuine Article#: YN401 Number of References: 19
Title: A switched virtual-GND level technique for fast and low power SRAM's
Author(s): Shibata N (REPRINT)
Corporate Source: NIPPON TELEGRAPH & TEL PUBL CORP,SYST ELECT LABS/ATSUGI/KANAGAWA 24301/JAPAN/ (REPRINT)
Journal: IEICE TRANSACTIONS ON ELECTRONICS, 1997, VE80C, N12 (DEC), P 1598-1607
ISSN: 0916-8524 Publication date: 19971200
Publisher: IEICE-INST ELECTRONICS INFORMATION COMMUNICATIONS ENG, KIKAI-SHINKO-KAIKAN BLDG MINATO-KU SHIBAKOEN 3 CHOME, TOKYO 105, JAPAN
Language: English Document Type: ARTICLE
Geographic Location: JAPAN
Subfile: CC ENGI--Current Contents, Engineering, Computing & Technology
Journal Subject Category: ENGINEERING, ELECTRICAL & ELECTRONIC
Abstract: Fast and low-power circuit techniques suitable for size-configurable SRAM macrocells are described. An SRAM cell architecture using virtual-GND lines along bitlines is proposed; each virtual-GND line switches the potential by inner read-enable and column-address-decoded signals. Reducing the active power dissipation in the memory **array** and shortening the time for writing data are simultaneously accomplished. The range of available supply voltages is enhanced by adoptive higher virtual-GND level control with a simple voltage limiter. An SRAM-macrocell rest chip is designed and fabricated with 0.5-mu m, CMOS technology. A 4K-word X 6-bit organization SRAM demonstrates 186-MHz operation at a 3.3-V typical power supply. Its power dissipation at a practical operating frequency, 100-MHz, is reduced to 29% (25-mW) by the proposed virtual-GND line techniques.
Descriptors--Author Keywords: SRAM ; low power ; **virtual** GND ; **column** address ; synchronous ; macrocell
Identifiers--KeyWord Plus(R): STATIC RAM; CMOS SRAM; ARCHITECTURE
Cited References:
DOUSEKI T, 1995, P107, P C MICR TEST STRUCT
HIROSE T, 1990, V25, P1068, IEEE J SOLID-ST CIRC
INO M, 1996, P86, ISSCC FEB
KONDO T, 1996, V16, P51, IEEE MICRO
MATSUMIYA M, 1992, V27, P1497, IEEE J SOLID-ST CIRC
MINATO O, 1979, V26, P882, IEEE T ELECTRON DEV
MIZUNO H, 1995, P25, 1995 S VLSI CIRC DIG
OHKUBO N, 1994, P599, P CICC
SHIBATA N, 1995, ICD95171 IEICE
SHIBATA N, 1995, V78, P473, IEICE T C
SHIBATA N, 1996, V79, P1120, IEICE T ELECT
SHIBATA N, 1993, V76, P1641, IEICE T ELECT C
SHIBATA N, 1995, V78, P570, IEICE T J
SHIBATA N, 1996, V79, P1171, IEICE T J
TRAN H, 1996, P68, S VLSI CIRC MAY
WATANABE T, 1983, P60, ISSCC FEB
YAMAUCHI H, 1996, P126, S VLSI CIRC MAY
YANO T, 1978, V61, P273, IEICE T C
YOSHIMOTO M, 1983, V18, P479, IEEE J SOLID-ST CIRC

24/5/11 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02652077 JICST ACCESSION NUMBER: 96A0056140 FILE SEGMENT: JICST-E
A Low-power Synchronous SRAM Macrocell with Column **-address Controlled** Virtual **-GND lines.**
SHIBATA NOBUTARO (1); WATANABE MAYUMI (1)
(1) Nippon Telegr. and Teleph. Corp., LSI Lab.
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 1995, VOL.95,NO.379(SDM95 155-162), PAGE.45-52, FIG.10, TBL.1, REF.5
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.2/.3.049.77 681.327
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: Circuit techniques for low-power and fast SRAM macrocells were described. A low-power memory cell with a virtual-GND line whose level was controlled by column-select signals and a WE-signal was proposed. A fast write scheme with above memory cells was also mentioned. A current-mode fast sense amplifier was devised to improve its switching speed. A synchronous SRAM-macrocell test chip was designed and fabricated with 0.5-.MU.m single-polysilicon double-metal CMOS technology. The low static-power of 360-.MU.A/bit and 190-MHz operation at 3.3-V were demonstrated by 4K-word SRAM's. (author abst.)
DESCRIPTORS: SRAM; macrocell; consumed electric power; speedup; earth(ground connection); data writing; data reading; voltage control; sense amplifier; switching; CMOS structure; integrated circuit memory; **array** circuit; ASIC
BROADER DESCRIPTORS: RAM; memory(computer); equipment; static memory; module; electric power; modification; improvement; data processing; information processing; treatment; electric quantity control; control; amplifier; MOS structure; device structure; semiconductor memory; circuit; integrated circuit; micro circuit
CLASSIFICATION CODE(S): NC03162T; JC04060F

File 344:Chinese Patents Abs Jan 1985-2006/Jan
(c) 2006 European Patent Office
File 347:JAPIO Dec 1976-2005/Dec(Updated 060404)
(c) 2006 JPO & JAPIO
File 350:Derwent WPIX 1963-2006/UD=200662
(c) 2006 The Thomson Corporation
File 371:French Patents 1961-2002/BOPI 200209
(c) 2002 INPI. All rts. reserv.

Set	Items	Description
S1	31	AU=(BUTZ D? OR BUTZ, D?)
S2	2	S1 AND (MATRIX OR MATRICES OR ARRAY? ? OR TABLE? ? OR ROW? ?(3N)COLUMN? ?)
S3	2	S1 AND ADDRESS?
S4	1	S1 AND IC=G06F
S5	2	S2:S4

5/5/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0013315319 - Drawing available
WPI ACC NO: 2003-402488/
Related WPI Acc No: 2002-404068
XRPX Acc No: N2003-321091
Matrix addressing **system for e.g. video display, has serially-connected** addressable **switches located to establish unique** array addresses **based on the state of the serially connected switches**
Patent Assignee: BUTZ D E (BUTZ-I)
Inventor: **BUTZ D E**
Patent Family (3 patents, 97 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
US 20030046508	A1	20030306	US 2000226100	P	20000817	200338	B
			US 2001932467	A	20010817		
WO 2003079363	A1	20030925	WO 2002US7317	A	20020312	200373	NCE
AU 2002254166	A1	20030929	AU 2002254166	A	20020312	200437	NCE
			WO 2002US7317	A	20020312		

Priority Applications (no., kind, date): AU 2002254166 A 20020312; WO 2002US7317 A 20020312; US 2000226100 P 20000817; US 2001932467 A 20010817

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 20030046508	A1	EN	38	20	Related to Provisional US 2000226100
WO 2003079363	A1	EN			

National Designated States,Original: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CN CO CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZW
Regional Designated States,Original: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW
AU 2002254166 A1 EN PCT Application WO 2002US7317
Based on OPI patent WO 2003079363

Alerting Abstract US A1

NOVELTY - **Addressing** layers include two types of **addressable** switches (202,204), each of which is responsive to at least two types of switching signals capable of transmission through the **addressing** layers. Serially connected **addressable** switches are located to establish unique **array addresses** based on the state of the serially connected switches.

DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

1.a matrix of uniquely addressable locations; and

2.a matrix of discretely addressable locations.

USE - For e.g. video display.

ADVANTAGE - Reduces inherent delay of reading and writing over narrow extended pathways.

DESCRIPTION OF DRAWINGS - The figure shows the example of a virtual column.

202,204 **Addressable** switches

Title Terms/Index Terms/Additional Words: **MATRIX** ; **ADDRESS** ; SYSTEM;

5/5/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0012458145 - Drawing available
WPI ACC NO: 2002-404068/200243
Related WPI Acc No: 2003-402488
XRPX Acc No: N2002-317166
Data storage device for video imaging system has virtual column connected to addressing **layer such that** addressable **switch elements are in conductive relationship with** addressing **layer**
Patent Assignee: BUTZ D E (BUTZ-I)
Inventor: **BUTZ D E**
Patent Family (2 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
US 20020041525	A1	20020411	US 2000226100	P	20000817	200243	B
			US 2001851887	A	20010509		
US 6462977	B2	20021008	US 2001851887	A	20010509	200269	E

Priority Applications (no., kind, date): US 2000226100 P 20000817; US 2001851887 A 20010509

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 20020041525	A1	EN	41	20	Related to Provisional US 2000226100

Alerting Abstract US A1

NOVELTY - The data storage device has at least one virtual column (300) having data storage elements (316,318) and **addressable** switch elements (304,306,308). The virtual column is connected to at least one of the **addressing** layers (310,312,314) such that the **addressable** switch elements are in a conductive relationship with the **addressing** layer.

DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

1.Memory; and

2.Data accessing method in a data storage device.

USE - Data storage device such as memory (claimed) e.g. read only memory (ROM), random access memory (RAM), DRAM, magnetic and optical disk, for computer, real-time video display device, video imaging systems, sensor **arrays** and logical processors.

ADVANTAGE - Requires lesser number of **address** bits and significantly reduces propagation delays in memory devices. Eliminates need for an interface between the central processing unit and memory device, and prevents need of **addressing** the **column** and **row** .

DESCRIPTION OF DRAWINGS - The figure shows two virtual columns connected to several **addressing** layers.

300 Virtual column
304,306,308 **Addressable** switch elements
310,312,314 **Addressing** layer
316,318 Data storage elements

Title Terms/Index Terms/Additional Words: DATA; STORAGE; DEVICE; VIDEO; IMAGE; SYSTEM; VIRTUAL; COLUMN; CONNECT; **ADDRESS** ; LAYER; SWITCH; ELEMENT; CONDUCTING; RELATED

Class Codes
International Classification (Main): G11C-029/00, G11C-005/06

```
File   2:INSPEC 1898-2006/Sep W3
         (c) 2006 Institution of Electrical Engineers
File   6:NTIS 1964-2006/Sep W4
         (c) 2006 NTIS, Intl Cpyrght All Rights Res
File   8:Ei Compendex(R) 1970-2006/Sep W4
         (c) 2006 Elsevier Eng.  Info. Inc.
File  20:Dialog Global Reporter 1997-2006/Oct 02
         (c) 2006 Dialog
File  23:CSA Technology Research Database 1963-2006/Sep
         (c) 2006 CSA.
File  34:SciSearch(R) Cited Ref Sci 1990-2006/Sep W4
         (c) 2006 The Thomson Corp
File  35:Dissertation Abs Online 1861-2006/Sep
         (c) 2006 ProQuest Info&Learning
File  65:Inside Conferences 1993-2006/Oct 02
         (c) 2006 BLDSC all rts. reserv.
File  94:JICST-EPlus 1985-2006/Jun W4
         (c)2006 Japan Science and Tech Corp(JST)
File  95:TEME-Technology & Management 1989-2006/Sep W4
         (c) 2006 FIZ TECHNIK
File  99:Wilson Appl. Sci & Tech Abs 1983-2006/Jul
         (c) 2006 The HW Wilson Co.
File 111:TGG Natl.Newspaper Index(SM) 1979-2006/Sep 18
         (c) 2006 The Gale Group
File 144:Pascal 1973-2006/Sep W2
         (c) 2006 INIST/CNRS
File 256:TecInfoSource 82-2006/Jan
         (c) 2006 Info.Sources Inc
File  56:Computer and Information Systems Abstracts 1966-2006/Sep
         (c) 2006 CSA.
File  57:Electronics & Communications Abstracts 1966-2006/Sep
         (c) 2006 CSA.
File  68:Solid State & Superconductivity Abstracts 1966-2006/Sep
         (c) 2006 CSA.
File  60:ANTE: Abstracts in New Tech & Engineer 1966-2006/Sep
         (c) 2006 CSA.
File 293:Engineered Materials Abstracts 1966-2006/Sep
         (c) 2006 CSA.
File 239:Mathsci 1940-2006/Nov
         (c) 2006 American Mathematical Society

Set     Items   Description
S1         78   AU=(BUTZ D? OR BUTZ, D?)
S2          2   S1 AND (MATRIX OR MATRICES OR ARRAY? ? OR TABLE? ? OR ROW?
                 ?(3N)COLUMN? ?)
S3          0   S2 AND ADDRESS?
```

File 345:Inpadoc/Fam.& Legal Stat 1968-2006/UD=200639
(c) 2006 EPO

Set	Items	Description
S1	1	PN=US 20030046508

1/39/1
DIALOG(R)File 345:Inpadoc/Fam.& Legal Stat

17749705
Basic Patent (No,Kind,Date): US 20020041525 AA 20020411 <No. of Patents: 003>
Patent Family:

Patent No	Kind	Date	Applic No	Kind	Date	
US 20020041525	AA	20020411	US 851887	A	20010509	(BASIC)
US 20030046508	AA	20030306	US 932467	A	20010817	
US 6462977	BB	20021008	US 851887	A	20010509	

Priority Data (No,Kind,Date):
US 851887 A 20010509
US 226100 P 20000817
US 932467 A 20010817

PATENT FAMILY:
UNITED STATES OF AMERICA (US)
Patent (No,Kind,Date): US 20020041525 AA 20020411
Patent Assignee: BUTZ DAVID EARL (US)
Author (Inventor): BUTZ DAVID EARL (US)
Priority (No,Kind,Date): US 851887 A 20010509; US 226100 P 20000817
Applic (No,Kind,Date): US 851887 A 20010509
National Class: * 365200000
IPC: * G11C-029/00; G11C-0005/02; G11C-0005/06; G11C-0008/00
Language of Document: English
Patent (No,Kind,Date): US 20030046508 AA 20030306
System and methods for addressing a matrix (English)
Patent Assignee: BUTZ DAVID EARL (US)
Author (Inventor): BUTZ DAVID EARL (US)
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